

ΔE/DX AND E/DX PIXELATED DETECTOR WITH MULTI-GUARD RINGS

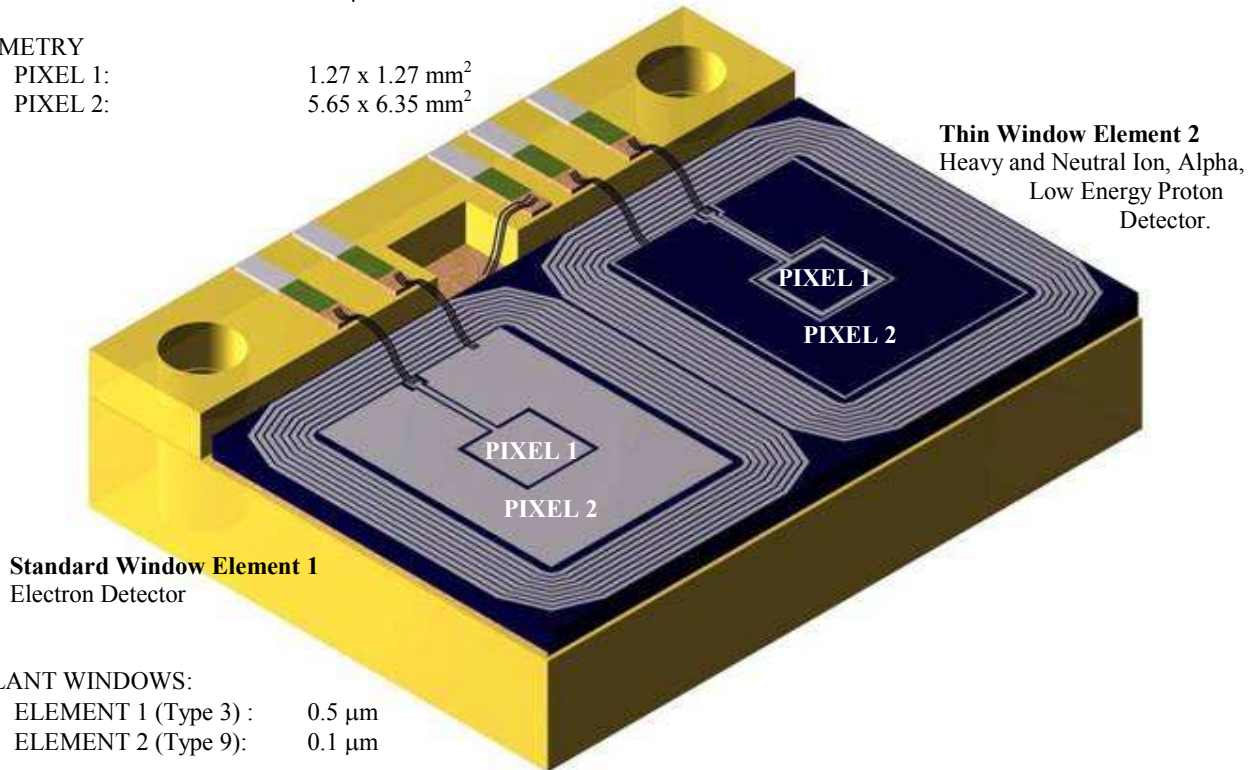
SILICON DETECTOR TYPE: DC coupled ion implanted totally depleted silicon pixelated detector.

TECHNOLOGY: 4 inch wafer technology.

DESIGN: Single sided pixelated device with a multi-guard ring design for high radiation environment operation.

THICKNESS: 500 μm

GEOMETRY
 PIXEL 1: 1.27 x 1.27 mm²
 PIXEL 2: 5.65 x 6.35 mm²



IMPLANT WINDOWS:
 ELEMENT 1 (Type 3) : 0.5 μm
 ELEMENT 2 (Type 9): 0.1 μm

FULL DEPLETION (FD): <100 V
 OPERATING VOLTAGE: FD to FD + 30 V

ELEMENT 1 LEAKAGE CURRENT: 25 nA
 ELEMENT 2 LEAKAGE CURRENT: 25 nA
 TOTAL LEAKAGE CURRENT: 50 nA
 ALPHA RESOLUTION ELEMENT 2: 12 KeV FWHM

METALLISING:
 ELEMENT 1: 10,000 Å over active area
 ELEMENT 2: 3000 Å around periphery of active area

PACKAGE: The chip is recessed in a non-transmission FR4 PCB
 Dimensions = 14.9 x 11.5 x 4.4 mm³
 Mounting holes, Ø 1.6 mm, are separated by 12.0 mm
 Solder pads

MINIMUM ACCEPTANCE LEVEL: 100 %
 EXPERIMENTS: MERCURY MESSENGER

QUALITY ASSURANCE :ISO9001

